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S. Y. B. Sc. (Electronics) (Sem. - III) Examination

March - 2023

Electronics : Paper - IV

Advance Digital Electronics and Circuits Design

[Total Marks: 50

સૂચના : / Instructions

(1)

નીચે દર્શાવેલ ☛ નિશાનીવાળી વિગતો ઉત્તરવહી પર અવશ્ય લખવી.
Fill up strictly the details of ☛ signs on your answer book

Name of the Examination:

☛ **S. Y. B. Sc. (Electronics) (Sem. - III)**

Name of the Subject :

☛ **Electronics : Paper - IV Advance Digital Electronics and Circuits Design**

Subject Code No.: **1903000203020092**

Seat No.:

Student's Signature

(2) Figure on the right indicates full marks
(3) All symbols and abbreviations have their usual meaning.
(4) Non-programmable calculators are allowed.
(5) Assume data if necessary.

***O.M.R. Sheet* ભરવા અંગેની અગત્યની સૂચનાઓ આપેલ *O.M.R. Sheet*ની પાછળ છાપેલ છે.**
Important instructions to fillup O.M.R. Sheet are given on back side of the provided O.M.R. Sheet.

Q. 1. Multiple Choice Questions: (1 Mark) 12

1. If an active-HIGH S-R latch has a 0 on the S input and a 1 on the R input and then the R input goes to 0, the latch will be _____.

   a) SET b) RESET

   c) Clear d) Invalid

2. Which of the following is correct for a gated D flip-flop?

   a) The output toggles if one of the inputs is held HIGH.

   b) Only one of the inputs can be HIGH at a time.

   c) The output complement follows the input when enabled.

   d) Q output follows the input D when the enable is HIGH.

3. Register that shift the information is called

   a) Latch b) Counter

   c) Shift register d) Flip-flop

4. An active-HIGH input S-R latch has a 1 on the S input and a 0 on the *R* input. What state is the latch in?

   a) $Q = 1, \overline{Q} = 0$ b) $Q = 1, \overline{Q} = 1$

   c) $Q = ?, \overline{Q} = 1$ d) $Q = ?, \overline{Q} = 0$

5. What is one disadvantage of an S-R flip-flop?

   a) It has no enable input. b) It has an invalid state.

   c) It has no clock input. d) It has only a single output.

6. The number of cells in a K-map with n-variables.

   a) 2n b) n^2

   c) 2^n d) n

7. The full form of SR is _____.

a) System rated b) Set reset

c) Set ready d) Set Rated

8. In down counter, _____ output of the first FF is connected to the clock input of the next FF.

a) Q b) $\overline{Q}$

c) CLK d) Vcc

9. The advantage of a J-K flip-flop over an S-R FF is that _____.

a) It has fewer gates b) It has only one output

c) It has no invalid states d) It does not require a clock input

10. Which of the following combinations cannot be combined into K-map group?

a) Corners in the same row b) Corners in the same column

c) Diagonal d) Overlapping combinations

11. When both inputs of SR latches are low, the latch _____.

a) Q output goes high

b) Q' output goes high

c) It remains in its previously set or reset state

d) It goes to its next set or reset state

12. A negative edge-triggered flip-flop will accept inputs only when the clock _____.

a) Is LOW b) Changes from HIGH to LOW

c) Is HIGH d) Changes from LOW to HIGH

Q. 2. Multiple Choice Questions: (2 Marks) 20

13. How many truth table entries are necessary for a four-input circuit?

a) 4 b) 8

c) 12 d) 16

14. Which of the following is a correct SOP expression?

a) (A+B)(C+D) b) (A) B (CD)

c) AB + CD d) AB(CD)

15. How many flip-flops are required to make a MOD-20 binary counter?

a) 3 b) 32

c) 5 d) 6

16. The terminal count of a decade counter is _____.

a) 1010 b) 1000

c) 1001 d) 1100

17. The min term when X=Y=Z=0 is _____.

a) $x'+y'+z'$ b) xyz

c) $x'y'z'$ d) x+y+z

18. How many flip-flops are required to construct a decade counter?

a) 10 b) 8

c) 5 d) 4

19. $A \cdot \overline{A}$ is equal to

a) 0 b) 1

c) A d) None of the above

20. How many clock pulses will be required to completely load serially a 5-bit shift register?

a) 2 b) 3

c) 4 d) 5

21. What type of register would have a complete binary number shifted in one bit at a time and have all the stored bits shifted out one at a time?

a) Parallel-in, parallel-out b) Parallel-in, serial-out

c) Serial-in, parallel-out d) Serial-in, serial-out

22. Full adder performs addition on

a) 2 bits b) 3 bits

c) 4 bits d) 5 bits

Q. 3. Multiple Choice Questions: (3 Marks) 18

23. A decimal counter has

a) 2 states b) 8 states

c) 10 states d) 16 states

24. With a 10 kHz clock frequency, eight bits can be serially entered into a shift register in _____.

a) 8 μs b) 80 μs

c) 800 μs d) 0.8 ms

25. Parallel loading is done with

a) 1 cycle b) 2 cycle

c) 3 cycle d) 4 cycle

26. A(A + B) = ?

a) A b) 1

c) (1 + AB) d) AB

27. Which of the following groups of logic devices would be the minimum required for a MOD-64 synchronous counter?

a) Five flip-flops, three AND gates

b) Seven flip-flops, five AND gates

c) Four flip-flops, ten AND gates

d) Six flip-flops, four AND gates

28. UP counter increment the value by

a) 1 b) 2

c) 3 d) 4

SPACE FOR ROUGH WORK